REMARKS

Claims 1-21 are pending in this application, of which claim 1 has been amended. No new claims have been added.

Claims 1, 7-9, 14 and 21 stand under 35 USC §102(e) as anticipated by Applicants' Admitted Prior Art shown in Figs. 1-3 (hereinafter "**APA**").

APA discloses a conventional synchronous rectification-type DC/DC converter, which comprises a control circuit 2 found on a single semiconductor integrated circuit substrate and seven elements 3 to 9 mounted externally. Control circuit 2 includes an idle period setting circuit 14 including fire inverter circuits 21 to 25, two transistors T1 and T2, two power suppliers 26 and 27 and two capacitors C1 and C2.

Page 5, lines 7-20 of the specification disclose:

> Preferably the DC/DC converter 1 operates on a low supply voltage in order to reduce power consumption. The idle period setting circuit 14, however, generates the first control signal S4 which has a pulse width smaller than that of the pulse signal S3 by the delay time td1. Accordingly, as shown in Fig. 4, an ON-duty ratio of the first control signal S4 with respect to the voltage of the error signal S1 becomes smaller than that of ideal characteristics. Therefore, it is impossible to set the duty ratio of the first control signal S4 (i.e., the first drive signal SG1) to a high value (for example, a value in the vicinity of 100%). For this reason, in the conventional DC/DC converter 1, it is difficult to lower the supply voltage to reduce the power consumption.

It should be noted that, although the Examiner has urged that the first drive signal (S4 of Fig. 3) has substantially the same pulse width as that of pulse signal (S3 of fig. 3), the quoted portion of the specification discloses that first control signal S4 "has a pulse width smaller than

that of the pulse signal S3 by the delay time td1." Thus, **APA** does not disclose generating the first drive signal having substantially the same pulse width as that of an input pulse signal, as recited in claims 1, 7, 14 and 21 of the instant application.

Thus, the 35 USC §102(e) rejection should be withdrawn.

Claims 2 and 5 stand under 35 USC §103(a) as unpatentable over **APA** in view of U.S. Patent 6,396,250 to Bridge (hereinafter "**Bridge**").

Applicants respectfully traverse this rejection.

The Examiner has urged that **Bridge** teaches a dc/dc converter having a drive signal generation circuit pulse signal wherein a second drive signal (G_2) that has a larger pulse width than a first drive signal (IN or G_1) using the pulse signal and the first drive signal.

Applicants respectfully disagree.

As shown in Fig. 18b, **Bridge** generates a signal G1 having a pulse width smaller than that of an input signal IN.

Thus, **Bridge**, like **APA**, fails to disclose generating the first drive signal having substantially the same pulse width as that of an input pulse signal, as recited in claims 1 and 14, from which claims 2 and 15 respectively depend.

Thus, the 35 USC §103(a) rejection should be withdrawn.

Claims 3, 10, 16 and 20 stand under 35 USC §103(a) as unpatentable over **APA** in view of U.S. Patent Publication 2004/0104714 to Nishimaki (hereinafter "**Nishimaki**").

Applicants respectfully traverse this rejection.

Nishimaki does not disclose generating the first drive signal having substantially the same pulse width as that of an input pulse signal. As shown in Fig. 8, **Nishimaki** discloses generating a pulse signal SH via the inverters 324 and 325 by providing a PWM signal and an output signal of the inverter 326 (pulse signal SL) to the NAMD circuit 312 and generating a pulse signal SL via the inverter 327 by providing the PWM signal, the pulse signal SH, and a detection signal NOFF to the NAND circuit 322. However, because the pulse signals SH and SL are provided to the inverters 322 and 321, respectively, **Nishimaki** cannot generate a pulse signal having substantially the same pulse width as that of the PWM signal, as recited in the claimed invention.

Thus, the 35 USC §103(a) rejection should be withdrawn.

Claims 4, 11 and 17 stand rejected under 35 USC §103(a) as unpatentable over **APA** and **Nishimaki** in view of **Bridge**.

Applicants respectfully traverse this rejection.

As noted above, **Nishimaki**, **APA** and **Bridge** all fall to teach the limitations of claims 1, 7 and 14, from which these claims respectively depend, and the 35 USC §103(a) rejection should be withdrawn.

Claims 5, 12 and 18 stand rejected under 35 USC §103(a) as unpatentable over **APA**, **Nishimaki** and U.S. Patent 4,862,364 to Matsuda.

Applicants respectfully traverse this rejection.

As noted above, **APA** and **Nishimaki** both fail to teach, mention or suggest the features recited in claims 1, 7 and 14, from which these claims depend. Thus, the 35 USC §103(a) rejection should be withdrawn.

Claims 6, 13 and 19 stand rejected under 35 USC §103(a) as unpatentable over **APA** and **Nishimaki** in view of U.S. Patent 6,577,517 to Jain et al.

Applicants respectfully traverse this rejection.

As noted above, **APA** and **Nishimaki** fail to teach, mention or suggest the features recited in claims 1, 7 and 14, from which these claims respectively depend. Thus, the 35 USC §103(a) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, claims 1-21, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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